Some information about the Matrix 6 key-scan circuitry R Grieb 2/2020

Since the CPU in the Matrix 6 is kept pretty busy updating the voices, Oberheim designed a dedicated circuit for scanning the keybed and measuring key velocity, instead of doing it in the main CPU or adding a second CPU. Here is some information related to the operation of this circuit. (This is just my understanding and may contain errors.)

Basic circuit timing is created by dual JK flip flop U40. The two timing signals C1 and C2 are 90 degrees out of phase and have periods of 4 uSec. By combining true and inverted versions of these signals, a number of different timing strobes are generated which control the sequence of events. (See timing sketch at bottom)

The low six outputs of counter U39 count through 64 different addresses of the three 1K by 4 SRAM chips. Only 64 of the 1024 addresses are used. Each address in the RAM corresponds to a key on the keybed, so the keys would be numbered 0-60 in this case, and the top three RAM addresses are not used, since there are only 61 keys. Every 4 uSec, counter U39 increments, selecting the location for the next key. RAM's U24, 31, and 38 are read and new data is written to them before the address increments again. The data read from RAMs U24 and U31 is loaded into counters U25 and U32. Two bits from U38 are loaded into U29. Since U39 increments every 4 uSec, each key's address comes around once every 64 counts, or every 256 uSec.

Electrically, the keybed is arranged into 8 groups of 8 keys. Each key has two switch contacts. All 16 switches in a group have one end tied together and this signal is driven low to scan these 8 keys. The other ends of the switches are pulled up through resistors, and will only be low if the switch is closed. When a key is pressed, one contact closes first, and then the second one closes. The time between the two closures indicates how fast the key was pressed, and this is what the circuit measures.

The low three RAM address bits are also applied to decoder U45 which drives one of the 8 key rows low. The upper three RAM address bits are fed to 8:1 muxes U44 and U43 which select one of the 8 keys in each row. So at any given time, one end of a group of 8 keys (one row) is driven low by U45 and U46. At the same time, just one key's column signals are selected by U44 and U43 and appear at pin 14 of these chips. When the selected key is pressed, first U44 pin 14 will go high, then some time later U43 pin 14 will go high. The circuit measures the time from U44-14 going high to U43-14 high. It measures this separately for each key.

U29 is clocked every 4 uSec and registers the outputs of U44 and U43. These are fed to U30 pins 5 and 6. This XOR gate's output will go high when the two signals are different, so it will go high when only the first key contact is closed. This high level at U30-4 is fed through U33 pins 2 and 3 and is written to the SRAM U38 D0. U36 also gets the two registered key switch signals, and U36-3 goes high when both switches are closed.

If no key is pressed, U30-4 should be low so all U38 addresses should be written with D0 low at the end of each cycle. When U38 is read at the beginning of each cycle, D0 is low, which causes Q0 of U29 to be low. U29 pin 3 will be high, enabling U36 pin 8 to go high, resetting counters U25 and U32. The outputs of these two counters are written into RAMs U24 and U31, through U26 and U33, so when no key is pressed, all 61 key addresses of these chips should contain 0.

Now if we press key number 3 on the keybed, when U45, U44, and U43 select this key, first U30-4 will go high, writing a 1 into U38 D0. The next time this key's switches are selected (256 uSec later) the high level from U38 D0 will be read and will be registered by U29, sending Q0 high. RAM's U24 and U31 will also be read and their values loaded into counters U25 and U32. U29 pin 2 (Q0) high enables U42 pin 12 to go high (if the second switch is not pressed yet, so U30 pin 4 is still high) and U36 pin 11 will then go high, clocking the two counter chips. So as long as only the first switch for this key is closed, each time this key is selected, the counters will be loaded with the RAM value, will get incremented, and this value will then be written back into the RAM. So the RAM value at the address for this key will keep incrementing, counting how long only the first switch is closed. When the second switch closes, U30 pin 4 will go low when this key is selected, this will send U42 pins 2 and 12 low, and U36 pin 11 will stop incrementing the counter for this key.

When the second switch closes for a particular key, U36 pin 3 will be high when that key is selected. This will make U37 pin 11 high. This will feed through U33 pins 14 and 13, and will be written into U38 D1 at this address. Before this time, U37 pin 11 was low for this key, so D1 to U38 was always written as 0. So when U37 pin 11 first goes high, U29 pin 7 will be low, so U30 pin 3 will go high. This will enable U42 pin 6 to go high, strobing the counter values for this key into FIFO chips U27, 28, 34, and 35. But at the end of this cycle, U38 D1 will be written as 1, so the next time this key is selected, U29 pin 7 will be high, so U30 pin 3 will stay low. This insures that the counter data is only loaded into the FIFO chips once, when the second switch for the selected key is first registered by U29 as closed.

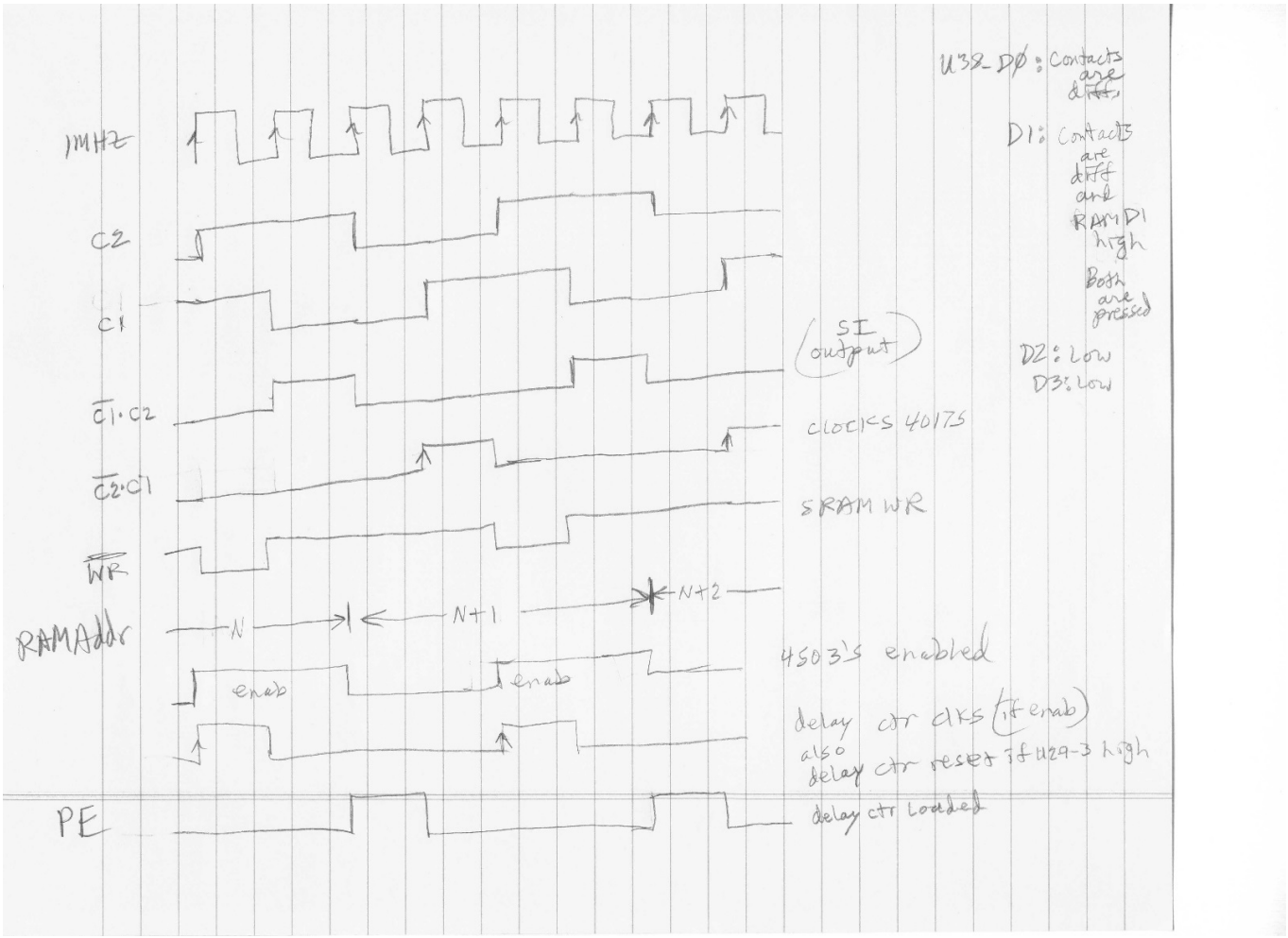
When the key counter value is strobed into the FIFO, the RAM address is also saved, to associate the counter value (velocity) with the correct key. Whenever there is data in the FIFO, the DOR signal from U27 will be high. Transitions on this signal cause the VIA chip U9 to generate an interrupt request to the 6809 CPU, which then reads the FIFO key press data.

When the key is released, after both contacts have opened, U37 pin 11 will go low with U29 pin 7 still high for one more cycle of the key addresses. This will generate a high level at U30 pin 3, and will load a key release message into the FIFO for this key. FIFO chip U35's D3 input indicates whether the FIFO data is for a key press or a release.

Despite what the schematic shows, it seems that 74C parts either were never used in this circuit, or were replaced with 74HC parts as time went on. Here are some part numbers taken from a Matrix 6 CPU board:

U36: 74HC08, U37: 74HC32, U39: 74HC393, U41: 74HC08, U42: 74HC11, U46:74HC244

The three SRAM locations were populated with TC5514AP-2 chips. This is a CMOS chip that is equivalent to the older 2114 NMOS part, but uses less power. It has a 200 nSec access time. One possible replacement would be type 6114 SRAMs, which are also CMOS. Probably the NMOS part would also work OK. SRAM U38 had failed in the Matrix 6 that I was helping to troubleshoot and replacing it fixed the issue.


1MHz
C2
C1
C1·C2
C2·C1
WR
RAMAddr
N
N+1
N+2
enab
enab
PE
U38_D0: Contacts are diff.
D1: Contacts are diff and RAM D1 high
Both are pressed
D2: Low
D3: Low
SI output
clocks 40175
SRAM WR
4503's enabled
delay ctr clks (if enab)
also delay ctr reset if U29-3 high
delay ctr loaded