Instructions for using the Prophet 5 Diagnostic Firmware

PLEASE READ CAREFULLY BEFORE INSTALLING!

The diagnostic software is in the form of a binary executable of 4 Kbytes. It fits into a single 2732 EPROM chip. If your Prophet has two 2732's installed, you can simply place the diagnostic EPROM in the U312 location and leave the other EPROM where it is.

It was written in Zilog Z80 assembly language and assembled with TASM32.

Note: Do not expect any patches in RAM to be preserved if you are running this code.

HW tests:

The following tests have been implemented:

a) Scratchpad RAM test
b) NVRAM 2K
c) NVRAM 1K
d) LED test
e) DAC tests
f) Oscillator calibration circuitry test
g) Sample and Hold Test
   The operation of these tests is intended to mimic the operation of the factory tests which were available at one time for the P5.

Simply power on the Prophet with the diagnostics EPROM installed to run the tests. You should see a "-" in the bank display digit. This is the main monitor section of the test code. From here you can enter one of the subgroups by pressing its number:

1) Memory tests. Displays "r" in program display digit.
2) LED test
3) DAC tests. Displays "d" in program display digit
4) Oscillator calibration circuit tests. Displays "c" in program display digit.
5) ADC/Pot Mux test. Displays "A" in program display digit.
6) Sample and Hold test. Displays "H" in program display digit.

Press 8 to exit a subgroup and return to the main monitor loop.

Memory tests

There are three memory tests.

Press 1 for scratchpad test, “S” on display

Press 2 for NVRAM 2K test, “b” for battery-backed RAM on display

Press 3 for NVRAM 1K test, “b.” on display

If a memory test fails, the failing bit(s) is displayed on the program LEDs. LED 1 is bit D0, LED 8 is bit D7.

NVRAM tests copy contents to scratchpad first, then test NVRAM, then copy back. If scratchpad is OK, then the contents of NVRAM should be preserved.

LED test

The LED test walks through all of the LED’s in rapid succession, one at a time. The LED test returns to the main monitor loop upon completion.

DAC tests

Press 1 to write 0000 to the DAC, U347-6 should be about 0V

Press 2 to write all 1’s to the DAC, U347-6 should be about 10.66V

Press 3 repeatedly to test individual DAC bits, one at a time. When bit 0 is set, the code displays a 1.

When bit 1 is set, the code displays a 2, etc. When bit 9 is set, the code displays an “A”, bit 10 shows “b”, bit 11 shows “c”, bit 12 shows “d”, and finally for bit 13 the code displays an “E”. On the next press of the “3” switch, the DAC is reset to all 0’s and the code returns to the DAC test subgroup. Note that the DAC actually has 16 bits, but the low two bits are always tied to ground. When we say “bit 0” we mean the lowest bit of the 14 that the CPU can actually write to.

Oscillator Calibration Circuit tests

Press 1 to test the Tune FF U322. Using U332, we first reset the flip flop and read its state using U323. We expect the flip flop Q to be low, and Qb to be high. If we don’t get the correct value, we turn on LED 1 and also LED 7, which simply indicates the test is finished. If the value is correct, we set the flip flop and read it again. This time if the value is not what we expect, we turn on 2 LED 2 and the LED 7. If both tests pass, we just turn on the LED 7. Press 7 to return to the Osc cal top level.

Press 2 to test the cycle counter and the total time counter, both of which are in the 8253, U315. First we preset the Tune FF so that Qb is low. CNTR EN is low. Now we write 2 to the cycle counter and 0 to the total time counter. Next we bring CNTR EN high. Then using preset and clear we drive the tune FF to clock the cycle counter once. This should cause its output to go low. We check for this. If the output of the cycle ctr is not low, we turn on LED 3 and LED 7 and wait for the 7 switch to be pressed. If the first test passes, we clock the cycle counter three times by forcing the flip flop. Now the cycle ctr output should be high, since we set the count to 2 and it counts down. We check for this and if we don’t see it, we turn on LED 4 and LED 7 and wait for 7 to be pressed. If the tests pass to this point, we check the total time counter, which should no longer be zero, just to see if it has incremented. If it is still 0, we turn on LED 5 and LED 7. If all tests pass, we just turn on LED 7 and wait for 7 to be pressed.

Press 3 to test the Tune Mux output clocking the tune flip flop. For this test, we write 0x2000 to the DAC, and enable the S&H to feed this value onto the OSC1A CV. We also select OSC1A at the Tune Mux and enable it. We clear the Tune flip flop. We then remove the clear signal and set the D input high. Next we wait for 40 mSec to allow the selected oscillator to clock the flip flop output high. Then we check to see if the flip flop output is high. If it is not, we turn on LED 6 and LED 7. When the 7 is displayed, the tune mux and the S&H should still be configured as they were during the test.

ADC/Pot Mux Test

In this test, the selected potentiometer voltage is continually being converted to a 7-bit digital value, which is then displayed on program LEDs 1-7, with 7 being the MSBit and 1 the least. Pressing 1 advances to the next potentiometer. Pressing 8 returns to the top level menu. It is normal for the binary value to not go all the way up to 7Fh. Potentiometers are selected in the following order, which is simply walking through the three chips that make up the Pot Mux:

1) Filter Attack
2) Filter Decay
3) Filter Sustain
4) Filter Release
5) Amp Attack
6) Amp Decay
7) Amp Sustain
8) Amp Release
9) Filter Cutoff
10) Filter Env Amt
11) Mix Osc B
12) Osc B PW
13) Mix Osc A
14) Osc A PW
15) Mix Noise
16) Filter Resonance
17) Glide
18) LFO Freq
19) WHMod Src Mix
20) PMod Osc B
21) PMod Flt Env
22) Osc A Freq
23) Osc B Freq
24) Osc B Fine

Then we go back to 1 again…

Sample and Hold Test

Since this test uses the DAC, you should insure that it's working properly first. In this test, the DAC is stepped through eight different channels and voltage values for each of the three 4051 mux chips. Each mux switch channel is enabled for 10 mSec, so the entire pattern repeats every 240 mSec, since there are 24 channels. (Actually, channel 8 of U355 is not used, but we select it anyway) So each capacitor is charged for 10 mSec, then must hold for 230 mSec. The Prophet code refreshes the caps at a much higher rate, like every 10-20 mSec, but I chose the slower rate to make any problems with droop more evident. The voltages at U357 should be 83.3mV + channel (0-7) times 333.3 mV. The voltages at U356 should be 166.7mV + channel (0-7) times 333.3 mV. The voltages at U355 should be 250mV + channel (0-7) times 333.3 mV. In other words the voltage at U362-7 should be 83.3mV. U363-7 should be ~416mV, etc. If you measure the voltages at the 4051 pins, the meter will discharge the cap some, so you will get lower values. You should measure at the outputs of the buffer op amps.

Press 8 to stop the test and return to the top level menu.

Here are the voltages you should measure, in mV. Don't be concerned if they are not exactly what is shown.

4051-X		U357		U356		U355
0	**U362-7**	83.3	**U360-7**	167	**U358-7**	250
1	**U363-7**	417	**U361-7**	500	**U359-7**	583
2	**U363-1**	750	**U361-1**	833	**U359-1**	917
3	**U362-1**	1083	**U360-1**	1167	**U358-1**	1250
4	**U354-1**	1417	**U352-1**	1500	**U350-1**	1583
5	**U353-7**	1750	**U351-7**	1833	**U349-1**	1917
6	**U354-7**	2083	**U352-7**	2167	**U350-7**	2250
7	**U353-1**	2416	**U351-1**	2500		